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Design and implementation of 16 X 16 Truncated multiplier with different families of Xilinx

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Abstract: *Multiplication and Squaring functions are widely used in many real time applications. They form an integral part in implementation of many Digital Signal Processing, Digital Image Processing and Multimedia algorithms. The size and power consumption of a DSP chip is influenced by the multiplication and squaring architectures that are used. The aim of this paper is to propose a novel fixed width, 16 bit parallel array multiplier. The proposed approach is aimed at providing a degree of flexibility to designers when it comes to designing fixed width multipliers with reduced area and delay. The design being proposed was implemented in Verilog, and simulation were carried out in Xilinx version 13.2.*

Keywords: *Digital signal processing(DSP), Bit truncation, Partial product reduction, Verilog HDL.*

I. Introduction

Multiplications are widely used in many real time applications. They form a very integral part in the implementation of many Digital Signal Processing, Digital Image Processing and Multimedia algorithms. The size, speed and power dissipation of any DSP chip can be significantly influenced by the design and implementation of its multiplication. This mandates the need to have a multiplication and squaring function that is not just fast but at the same time occupies less area on the chip.

Over the years lot of research has been done in designing and implementing multiplication functions that yield less area on the chip, consume less power and have minimal propagation time. The move towards achieving less area on chip started with the implementation of fixed width multipliers. There are many different approaches to deriving a fixed width multiplier. Firstly Truncating the 2n bit result of a full-width multiplier to generate a result which is n bits wide. The least significant n bits out of 2n bits are truncated. This design yields the best results of all the fixed-width multiplier designs. However, the area savings are minimal. This is mainly because the design retains all the columns of the partial product array even when generating a truncated output The second approach involves truncating the least significant n columns of the partial product matrix of a full-width multiplier to directly yield a result that is n bits wide. Multiplication are the main part in the implementation of any communication system modules like any kind of filters, digital circuits etc.

This brief is organized as follows. Section II discusses the Existing Multiplier scheme, III describes Proposed Truncated Multiplier scheme, how the bits are truncated and the scheme is finally reduced, IV compares the experimental results.

II. Existing Multiplication Schemes

The Existing multiplier uses the full width multiplier and parallel multiplier scheme. In a parallel multiplier all the partial product terms are generated in parallel and the final result is obtained by adding the partial product terms over the columns. For the addition of partial product bit the combinational circuits like Half adder and Full adder is been used. The figure shows the step by step procedure of partial products addition of full width multiplier.

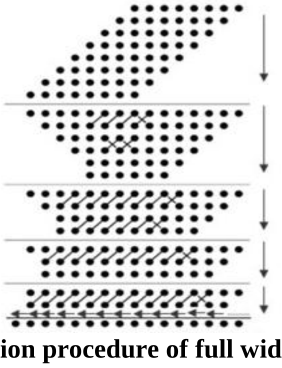

Fig 1: Addition procedure of full width multiplier

In a full width multiplier with an n-bit Multiplicand and an n- bit Multiplier, the output is a 2n-bit word. There are 2N- 1 columns in partial product array matrix and the terms are added column-wise to yield a 2n bit result. The presence of AND gates to generate the partial product terms and the HALF and FULL ADDERS to perform the column wise sum of the partial product terms results in large number of transistors. Hence, the large power consumption. This scheme of multiplication also uses more number of combinational circuits, since it has to add all the partial products bits both LSB and MSB.

III. Proposed Truncated Multiplier Scheme

This paper discuss the implementation of fixed width parallel multiplier with the truncation of LSB bits. During the truncation of partial products some amount of error is introduces in the generation of final output. In order to offset the error introduced due to truncation, a constant term is added to most significant N + K columns. This correction is the average of the truncated portion of the partial product matrix. The result obtained after adding the partial product terms is rounded to yield an N-bit result.

$$A = \sum_{i=0}^{n-1} a_i 2^{-n+i} \qquad (1)$$

$$B = \sum_{i=0}^{n-1} b_i 2^{-n+i} \qquad (2)$$

$$P = \sum_{i=0}^{2n-1} p_i 2^{-2n+i} \qquad (3)$$

Here A and B are the inputs an P is the partial product.

The error produced in the generation of final output of the truncated multiplier is mot more than 1 ulp(unit in the last place) so there is no need of any compression circuits in this design. The 1 ulp error can be minimized during the design of any DSP or any circuits. The proposed multiplier also reduces the number of Half adder as compared to Full adder since Full adder has high compression rate as compared to Half adder. The proposed multiplier uses the column by column reduction scheme so that the partial products are reduced in each column causing less number of components used.

The proposed multiplier scheme has used two different block for the addition and reduction of partial products, these are Half carry and the Full carry. These two blocks are very similar to that of Half and Full adder but the difference is that it do not produces the sum bits it just calculates the carry bits like other adder. In this way it reduces the use of gate components. Finally for the addition of products a carry propagation scheme has been used in the last step. The figure shows how the partial products bits has been reduced in the column by column manner.

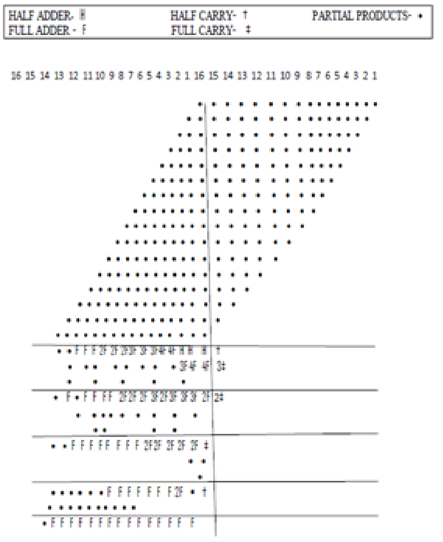

Fig 2: Reduction scheme of Proposed Truncated multiplier

The above figure shows hoe the lSB bits are truncated and finally the bits are reduced and the use of half carry and the full carry block.

A. ***Half Carry***

The half carry block are needed for the calculation of the last lsb bits such that it do not gives the sum part. The half carry block only generates the carry for the two bits as inputs. The half carry block comprises of the single AND gate. The internal structure of this block can be shown as:

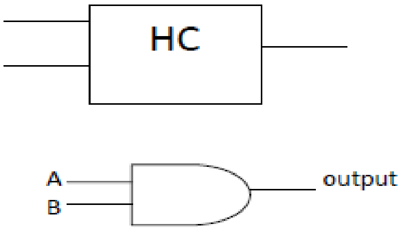

Fig 3: Block diagram and internal structure of Half carry

B. ***Full Carry***

As like half carry block full carry block also is used to calculate the last lsb bits in the truncated multiplier block. The full carry block also do not give any sum as output like full adder , it just provide the carry as output. Like full adder it has three bits as inputs and two bits as output. The full carry block is implemented using AND gate and OR gate. The internal structure of the full carry block is shown in figure below.

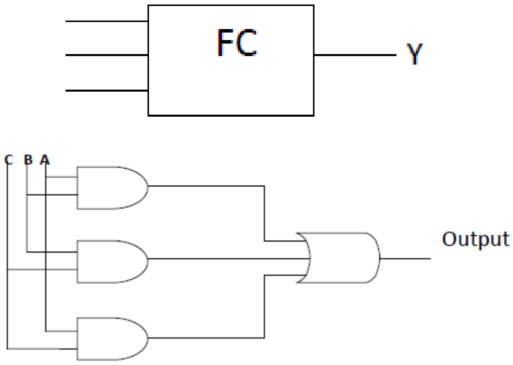

Fig 4: Block diagram and internal structure of Full carry

IV. Simulation Results

The Proposed multiplier block shows area as well as delay improvement as compared to the Existing fixed width multiplier. The existing multiplier block uses the full width calculation for the final output so it needed more number of internal blocks for the addition of bit. Hence requires more area than truncated multiplier block. Both the multiplier is simulated and synthesized using Xilinx 13.2 with family as Spartan 6. Following table shows the comparison of existing full width multiplier with proposed truncated multiplier.

Table I. Comparison Between Existing And Proposed Multiplier

Blocks	**No of LUTS**	**No. of Slices**	**IOBs**	**Delay(ns)**
Existing Full width Multiplier	238	132	48	28.76
Proposed Truncated Multiplier	202	112	48	26.88

When the proposed truncated multiplier is simulated using different families of Xilinx it gives different values of area and delay. The graph shows the number of slices used by the proposed truncated multiplier for different families of Xilinx.

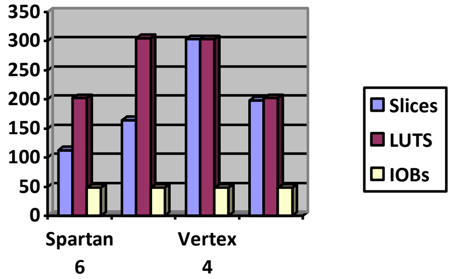

Fig 5: Area occupied by Truncated Multiplier in different families of Xilinx

V. Conclusion

This paper has presented a 16 bit Truncated multiplier which shows a considerable amount of reduction in the area as well as in the delay of the multiplier block. The proposed multiplier has also been implemented using different families of Xilinx like Spartan 6, Spartan 3, Vertex 4 and Vertex 6. Among all the families the Spartan 6 family of Xilinx shows the best area reduction in the implementation of 16 bit Truncate Multiplier.

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